Hack-A-Sat Flatsat Upgrade Instructions

The Hack-A-Sat team has made some upgrades since your initial flatsat delivery. Follow these instructions to upgrade your flatsat to the Finals game configuration. There will still be some differences from your team’s flatsat and the flatsat used in the finals competition. Namely a different radio is being used in the finals competition. In addition, the files provided do not include the challenge-specific software loads. These instructions are intended to put your flatsat into a configuration that mimics how the finals flatsat would operate in a nominal configuration.

Prerequisites:

* 2 x FTDI cables (LEON3 debug UART / cFS Console UART)
* USB to mini USB cable (for flashing FPGA bitstream to Ztex board Flash)
* USBasp (for flashing EyasSat boards)
* Obtain ztex files
  + https://www.ztex.de/downloads/ztex-191017.tar.bz2
* Obtain grmon
  + https://www.gaisler.com/index.php/downloads/debug-tools

Required Files:

* Cosmos installation
* cFS Install prom Image
  + core-cpu3.prom
* Eyassat Firmware Files
  + SubsystemADCS\_20200731.hex
* FPGA Bitstream
  + openMSP430\_fpga\_finals\_exp\_radio\_4\_teams.bit
* Payload SD Card Image
  + Payload\_SD\_Card.tar.gz

Initial Setup:

* Install Cosmos using steps from INSTALL.txt file
* Install avrdude
  + <http://download.savannah.gnu.org/releases/avrdude/avrdude-6.3-mingw32.zip>
* Install usbasp drivers – Can use Zadig according to instructions on this page
  + <https://www.fischl.de/usbasp/>
  + <https://electronics.stackexchange.com/questions/416714/avrdude-does-not-recognize-usbasp-device/417509#417509>
* Flash firmware to EyasSat ADCS board
  + Remove the EyasSat ADCS board from the board stack-up
  + Connect USBasp to ISP connector on the board
  + Apply 5V to the ADCS board
  + Flash the board
  + >avrdude.exe -C avrdude.conf -v -p atmega128 -c usbasp -U flash:w:SubsystemADCS\_20200731.hex:i
* Write FPGA bitstream to flash memory on Ztex board (using ztex SDK)
  + Connect USB cable to mini USB cable to Ztex board
  + Write bitstream to Ztex flash

$ cd ~/ztex/java/FWLoader/

$ sudo ./FWLoader -c -um openMSP430\_fpga\_finals\_exp\_radio\_4\_teams.bit

First free sector: 71

Writing sector 59 of 59

FPGA configuration time: 44360 ms

First free sector: 71

* Connect FTDI cables to Cromulence C&DH Board
  + See C&DH board schematic
  + Debug UART – J3 Connector

|  |  |  |
| --- | --- | --- |
| Gnd – Pin 2 | Tx – Pin 15 | Rx – Pin 13 |

* + cFS Console UART – SV1 Connector

|  |  |  |
| --- | --- | --- |
| Gnd – Pin 4 | Tx – Pin 1 | Rx – Pin 3 |

* + - Connect to Console through putty, minicom or screen
    - Baud rate is 38400
* Write cFS image to flash using Grmon
  + cd to grmon binary directory
  + launch grmon

$ cd <grmon install folder>/linux/bin64/

$ ./grmon -uart /dev/ttyUSB#

grmon3> spim flash detect

grmon3> spim flash erase

grmon3> spim flash load core-cpu3.prom

grmon3> run

* Verify cFS console output

